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EXAMINER	
SAXENA, AKASH	

ART UNIT	PAPER NUMBER
2128	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/673,467	STRANG, ERIC J.	
	Examiner	Art Unit	
	AKASH SAXENA	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-11,14-34,37,38,41-54 and 58-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-11,14-34,37,38,41-54 and 58-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/08/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-7, 9-11, 14-34, 37-38, 41-54, 58-60 has/have been presented for examination based on amendment filed on 10/19/2010.
2. A request for continued examination under 37 CFR 1.114 was filed in this application after a decision by the Board of Patent Appeals and Interferences, but before the filing of a Notice of Appeal to the Court of Appeals for the Federal Circuit or the commencement of a civil action. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 10/19/2010 has been entered.
3. Double Patenting rejection with applications 10/673,507, 10/673,501, 10/673,138, 10/673,583 is withdrawn in view of the Terminal Disclaimer filed 09/02/2008.
4. Claim(s) 1, 28 and 58 is/are amended.
5. Claim(s) 8, 12-13, 35, 39-40, 55-57 and 61 are cancelled.
6. Claim(s) 1-7, 9-11, 14-34, 37-38, 41-54, 58-60 are newly rejected under 35 USC § 112.
7. Claim(s) 1-7, 9-11, 14-34, 37-38, 41-54, 58-60 are newly rejected under 35 USC § 103.
8. The arguments submitted by the applicant have been fully considered. Claims 1-7, 9-11, 14-34, 37-38, 41-54, 58-60 are rejected and this action is made **Non-FINAL**. The examiner's response is as follows.

Inventorship Correction

9. Examiner has noticed that a correction of inventorship was filed in copending application 10673501. Applicant is encouraged to correct this issue in this application as well.

Claim Interpretation

10. Claim 1 discloses "spatially resolved model", however the disclosure appears to lack a definition what a spatially resolved model (See specification: [0037] [0098]) constitutes to gain better understanding of the claim. Further claim appears to indicate the have "spatially resolved model" as intended use of the "first principles simulation model" as in

"solving the computer-encoded differential equations of the first principles simulation model for the spatially resolved model in a time frame shorter in time than the actual process being performed;..."

Therefore no patentable weight is given to "spatially resolved model". Further if applicant intends to recite more positively the "spatially resolved model", two things are needed. First, a clear definition of the spatially resolved model with support from specification; Second, a recitation of connection to "first principles simulation model" (e.g. a type of "first principles simulation model") and how it meets the shorter time frame requirement for concurrent execution with the wafer process.

Response to Applicant's Remarks for 35 U.S.C. § 112

11. As per arguments made for enablement on Remarks Pgs. 20-24, using distributed simulation to address the enablement for the first principle simulation is not found to be persuasive because it still does not address updated & clarified rejections made below. Enhancement in real time simulation due to this networking (as shown in Remarks Pgs. 20-21) is not unexpected result (See Jain Section IV & V). Further this does not obviate what constitutes a first principle model and how it is faster than other known methods of simulation (at least see Sonderman: at least in Col.5 Lines 11-17; 49-67).

Response to Applicant's Remarks for 35 U.S.C. § 103

(Argument 1) Applicant has argued in Remarks Pg.18:

> The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation." United States v. Telectronics, Inc., 857 F.2d 778,785 (Fed. Cir. 1988).
>
> For the Examiner's consideration of what was known in the art at the time of filing,I attached is a 2002 article from Chemical Engineering Science entitled: "Visualization and numerical simulation of fine particle transport in a low-pressure parallel plate chemical vapor deposition reactor." This article on page 509 shows the use of spatially resolved model of the physical geometry of a parallel plate CVD reactor (i.e., set of 2,000,000 triangular/tetrahedral meshes). This article on page 499 indicates that the numerical simulations were performed using the commercially available CFD code Fluent 5.3 (Fluent, Inc.). Excerpts from this paper are reproduced below on the next page. While provided for the sake of showing that one of ordinary skill in the art would not have to use undue experimentation to make a spatially resolved model of a physical geometry of the semiconductor processing tool, this reference also does not show the use of solutions from such models being used for process control or being produced in a time frame consistent with that of a semiconductor manufacturing process. **[1]**

(Response 1) Examiner thanks applicant for mapping from the specification. However as pointed out in [1] above by application, there are two issues. First the specification does not disclose "first principles simulation model (computer encoded differential equations in claim limitation steps 1 and 4) for the spatially resolved model" and Secondly, "solving

... the spatially resolved model concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed...". For the first issue, the specification [0035] never discloses a "first principles simulation model for the spatially resolved model". At best it states physical model 106 may include a spatially resolved model. However no details of such model are disclosed and how it is the first principles simulation model. As per second issue the specification [0056] discloses (First principle) simulation may run slower the wafer process – therefore the even the First Principle simulation model is not disclosed as definitively running in a shorter time period. At the heart of the whole issue is not whether one of ordinary skill in the art can make or use the spatially resolved model but can one make of use a first principle simulation model for the spatially resolved model which runs in time frame shorter in time than the actual process being performed. Specification and cited art both lack this disclosure.

(Argument 2) Applicant has argued in Remarks Pg.25-26:

> There is no detail here of a spatially resolved model of a physical geometry of the semiconductor processing tool or the setting initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool.

(Response 2) Applicant's own remarks state: " One of ordinary skill in the art would know that a "spatially resolved model of a physical geometry of the semiconductor processing tool" is simply a model of the physical geometry of the tool using separated points in space.". Sonderman teaches equipment model to be a model of equipment (e.g. a furnace). Sonderman in Col.5 lines 62-67, which states:

> The e**quipment model 330 comprises components that can model furnace** behavior during semiconductor manufacturing processes. **The equipment model 330 can also model the *temperature response*, pressure response, and at other such characteristics** [1] relating to equipment that performs manufacturing processing.:

Applicant's own specification [0035] discloses the spatially resolved model to have these commonly known characteristics:

> [0035] First principles physical model 106 is a model of the physical attributes of the tool and tool environment as well as the fundamental equations necessary to perform first principles simulation and provide a simulation result for facilitating a process performed by the semiconductor processing tool. Thus, the first principles physical model 106 depends to some extent on the type of semiconductor processing tool 102 analyzed as well as the process performed in the tool. **For example, the physical model 106 may include a spatially resolved model of the physical geometry of the tool 102.** [a] which is different, for example, for a chemical vapor deposition (CVD) chamber and a diffusion furnace. **Similarly, the first principles equations necessary to compute flow fields are quite different than those necessary to *compute temperature fields.*** [b] The physical model 106 may be a model as implemented in commercially available software, such as ANSYS, of ANSYS Inc., Southpointe, 275 Technology Drive Canonsburg, PA 15317, FLUENT, of Fluent Inc., 10 Cavendish Ct. Centerra Park, Lebanon, NH 03766, or CFD-ACE+, of CFD Research Corp., 215 Wynn Dr., Huntsville, AL 35805, to compute flow fields, electro-magnetic fields, temperature fields, chemistry, surface chemistry (i.e. etch surface chemistry or deposition surface chemistry). However, special purpose or custom models developed from first principles to resolve these and other details within the processing system may also be used.

Examiner's teaching from Sonderman therefore teaches a spatially resolved model which teaches temperature response of the equipement model (See [1] and [a]-[b] from above. Applicant's own citation of Kee (US Patent No. 5583780 Col.3 Line38-65 and Col.6 Line 38- Col.7 Line 11 discloses a spatially resolved semiconductor tool/equipment model of known since 1996). Teaching of such a semiconductor equipment model in Sonderman (2004) is obvious over what is known in the art Kee (1996).

(Argument 3) Applicant has argued in Remarks Pg.25-26:

> There is once again no detail here of a spatially resolved model of a physical geometry of the semiconductor processing tool or the setting initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool.

> Moreover, statistical models, like Sonderman et al (and Tan et al), do no_.At have initial and boundary conditions, but rather are models which simply correlate inputs and outputs of a process based on statistical data from previous process runs. These models also do not solve for a variable over a gridded spatial domain, but instead use statistics to provide predictions about the end result that would be obtained if a process were run in a certain manner.

(Response 3) Applicant has argued that Sonderman and Tan teach statistical models - whereas applicant's claim do not expressly state the claim cannot have statistical inputs. Therefore the argument is not persuasive because Sonderman teaches initial and boundary conditions as predetermined specification and system definitions respectively of the equipment model. Specifically Sonderman Col.7 Lines 21-36 states:

> Turning back to FIG. 5, once the system 100 prepares the process models, the system 100 executes a simulation (block 520). In one embodiment, the simulation environment 210 executes the simulation. A more detailed description of the simulation execution described in block 520 is provided below. Once the system 100 executes the simulation, the system 100 makes a determination whether the results from the simulation are acceptable as compared with a predetermined specification (block 530). In other words, a determination is made, given a set of control parameters and system definitions, as to whether the device physics model 310, the process model 320, and the equipment model 330, when executed using the control parameters and definitions, produce a theoretical semiconductor wafer that contains electrical characteristics that are within a specific predetermined specification.

Arguments pertaining to data from manufacturing environment 170 and simulation environment 210 on pages 26-27 are considered however it is unclear how they relate to argument of initial and boundary condition as summarized on remarks Pg. 26-27. Further Chen used below teaches in Col.6 Lines 34-51 – simulation w/ actual process having initial (initialized parameter) and boundary (user defined parameters) conditions.

Further claim does not claim "gridded spatial domain" as argued by applicant.

(Argument 4) Applicant has argued in Remarks Pg.28-29:

> **Secondly**, Secondly, the combination of Sonderman et al and Jain et al is improper…

> Thus, as emphasized above, the proposed development work in Jain et al requires the development of futuristic computational equipment which one of ordinary skill in the art would be reluctant to implement or utilize for the rigorous standards needed in semiconductor manufacturing.
>
> ...
>
> As attested to in the declaration filed in related application U.S. Serial No. 10/673,507, with the computing capability of Jain et al representing futuristic, unrealized capabilites, there is no reasonable expectation of success that computer-encoded differential equations of a first plinciples simulation model for a spatially resolved model of a semiconductor processing tool could have been solved in a time frame shorter in time than the actual process being performed in the semiconductor processing tool.

(Response 4) Since, Jain (1994) and applicant's alleged reduction to technically realize the invention (~2002) computing capacity has nearly doubled every two years (Moore's Law), therefore one of the ordinary skill in the art in 2002 would not see the teaching of Jain as futuristic.

Applicant has provided no evidence to the contrary along with affidavit in the copending application of this disclosure to be so futuristic that it cannot be made or used. Applicant has not filed a similar affidavit with evidence in this application.

(Argument 5) Applicant has argued in Remarks Pg.30-31:

> **Thirdly**, Tan et al do not teach solving the computer-encoded differential equations of the first principles simulation model for the spatially resolved model concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed.
>
> The examiner in related application U.S. Serial No. 10/673,507 relied on Tan et al for their teaching of at col. 2, lines 7-10, of model-based real time process control using in situ inputs, process models, and process control strategies to correctly process control parameters during the process run. Yet, a "model-based" real time process control does not specify when the model is completed, only that the "process control" in Tan is real time and does not indicate that a solution to computer-encoded differential equations of the first principles simulation model for a spatially resolved model of a physical geometry of the semiconductor processing tool can be obtained in a time frame shorter in time than the actual process being performed.

(Response 5) The Examiner has no jurisdiction over issues decided by the board in the copending application 10/673,507 and makes no additional comment.

(Argument 6) Applicant has argued in Remarks Pg.31-32:

> Accordingly, Applicants resubmit that Tan et al do not disclose solving computer- encoded differential equations of the first principles simulation model for a spatially resolved model of a physical geometry of the semiconductor processing tool in a time frame shorter in time than the actual process being performed.
> ...
> Thus, Tan et al use post-process data to update and store a model for a subsequent processing step. It is the updated model (completed ahead of the next run) that is used to control the next process run, thereby providing the model-based real time process control during the process run.
>
> In other words, in Tan et al, the solution to the model exists prior to process control is not derived concurrently with the process control.
> ...

(Response 6) Allegation relating to update and store of the model does not negate the fact that in situ data is used as input to the model (e.g. from Tan Fig.2 Metrology machine #1 *204*). There is no requirement in claim that the model cannot be updated in subsequent simulation runs. Further even in Sonderman it is made clear that the model and model input are separate (Sonderman: Col.7 Lines 8-20). The solution is derived concurrently to and before the actual manufacturing as evident from Fig.2 and associated disclosure - See calculated processing parameter which are calculated from process model 202 when the process model gets the metrology data from the metrology machine #1 (204). Having an updated model does not impede with the teaching of the claim limitations and applicant has not provided any reason for it either. Therefore applicant's arguments are unpersuasive.

(Argument 7) Applicant has argued in Remarks Pg.33-34:

> Moreover, the previously filed declaration noted above attested to the fact that neither Sonderman et al nor Tan et al use a first principles simulation model. Rather, as attested to, the models in these references are 1) simplified models based on former approximate solutions or 2) statistical or "learned" models tracking how the systems are expected to behave.
> ....
> KSR Guidelines ....

(Response 7) Examiner does not see a declaration filed in this case pertaining to Tan. Further if applicant is referring to declaration filed in the copending application

10/673,507, a complete response to provided in respective file wrapper and arguments made there were unpersuasive. Examiner notes applicant's citation of KSR guidelines.

(Argument 8) Applicant has argued in Remarks Pg.34-36:

> Support for Applicants position is found in the following three references 1) U.S. Pat. No. 6,185,472; 2) U.S. Pat. No. 7,047,095; and 3) U.S. Pat. No. 6,587,744.
>
> ...
> The Office has provided no evidence of any solution times prior to the invention for the solving of computer-encoded differential equations of a first principles simulation model for a spatially resolved model of a physical geometry of the semiconductor processing tool.

(Response 8) Applicant's showing that other patents still teach longer simulation times as compared to wafer processing time, does not alleviate the fact that the applicant's disclosure seems to be silent on **how** *"solving the computer-encoded differential equations of the first principles simulation model for the spatially resolved model concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed".* Applicant own disclosure teaches longer simulation time periods for first principle simulation in specification [0056].

Tan reference in combination of Sonderman and Jain is provided as teaching the complete limitation. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

(Argument 9) Applicant has argued in Remarks Pg.36-37:

> **Fourthly**, in support of Applicants' position on the non-obviousness of the claims, the filed declaration in related application U.S. Serial No.10/673,507 attested to the fact that, prior to the filing of this application, a two-dimensional axisymmetric time-evolution temperature simulation of a chuck with a wafer, a plasma heat load, and a coolant heat removal was performed. By setting initial and boundary conditions to values appropriate for …

(Response 9) Applicant has not filed a similar affidavit with evidence in this application. A complete response to the affidavit is addressed in the respective application.

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Claim Rejections - 35 USC § 112¶1st

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

12. Claims 1-7, 9-11, 14-34, 37-38, 41-54, 58-60 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for *setting initial and boundary condition for first principle physical model*, does not reasonably provide enablement for *setting initial and boundary condition for a spatially resolved model of physical geometry of the semiconductor processing tool* as claimed in claim 1, 28 & 58. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. Applicant's disclosure in [0035] stating "physical model may include a spatially resolved model of the physical geometry of the tool" is not sufficient to meet the enablement requirement as applicant themselves admitted in [0035] that each model for CVD different from furnace. Dependent claims 2-7, 9-11, 14-27, 29-34, 37-38, 41-54, 59-60 are rejected as inheriting this deficiency respectively from claims 1 & 28.

13. Claims 1-7, 9-11, 14-34, 37-38, 41-54, 58-60 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for solving the computer-encoded differential equations of the first principles simulation model in a time frame shorter in time than the actual process being performed (Specification: [0056] [0057]), does not reasonably provide enablement for *solving the computer-encoded differential equations of the first principles simulation model for the spatially resolved*

model concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed; providing a first principles simulation result from the solution of the computer- encoded differential equations solved concurrently with the actual process being performed. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. The spatially resolved model (Specification: [0035]) is a type of model for a physical tool and is different for each tool as disclosed in the specification. Applicant has also shown that some simulation for the first principle model cannot be run concurrently with the wafer process and may take longer. There is no disclosure that this specific type of model (i.e. "spatially resolved model") can be run concurrently *in a time frame shorter in time than the actual [wafer] process being performed*.

Dependent claims 2-7, 9-11, 14-27, 29-34, 37-38, 41-54, 59-60 are rejected as inheriting this deficiency respectively from claims 1 & 28.

14. Claim 1-7, 9-11, 14-34, 37-38, 41-54, 58-60 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Exact details of what spatially resolved model as an example of first principle simulation model which is critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Applicant has quoted specification paragraphs [0035] and [0036]. These paragraph are not enabling, although they rely on the commercially available packages to

model the various first principle simulation models, the details of the spatially resolved model are absent from the specification. The details of these model which lead to unexpected results are very relevant to the designing the first principle physical model. Dependent claims 2-7, 9-11, 14-27, 29-34, 37-38, 41-54, 59-60 are rejected as inheriting this deficiency respectively from claims 1 & 28.

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Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

15. Claims 1-7, 9-11, 14-21, 23-34, 36-38, 41-48, 50-54, 58-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter), in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter), further in view U.S. Patent No. 6,263,255 issued to Tan et al (Tan hereafter).

Regarding Claim 1

Sonderman teaches a method of controlling a process performed by a semiconductor processing tool (**Sonderman**: Summary, at least in Col.2 Lines 10-17; Col.3 Lines 45-49), by ***inputting*** *a first principles physical model including a set*

of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool (**Sonderman**: at least in Col.5 Lines 11-17; 49-67) as device physics model, a process model and an equipment model.

Further, Sonderman *teaches **inputting** process data for an actual process being performed by the semiconductor processing tool* (**Sonderman**: at least in Col.3 Lines 50-67; *Col.7 Lines 8-20*). Further, Sonderman teaches setting initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool (**Sonderman**: Col.7 Lines 21-35) as predetermined specifications, **based** on the input data for the actual process being performed by the semiconductor processing tool (**Sonderman**: Col.7 Lines 7-20).

Sonderman does not teach first principle model including a set of computer encoded differential equations.

Jain teaches *solving* *the computer-encoded differential equations of the first principles simulation model* using MPE engine, which can be applied to wafer processing (**Jain**: Abstract; Pg. 372 Section V Dedicated MPE).

As stated earlier Sonderman teaches spatially resolved model(**Sonderman**: Col.7 Lines 21-35). Further, **Sonderman & Jain teaches *providing*** *a first principles simulation result process* (**Sonderman**: Fig. 1-3 *Col.7 Lines 4-7; Col.3 Lines 56-63*) *from the solution of the computer- encoded differential equations* (**Jain**: Abstract & Pg. 372 Section V Dedicated MPE) *solved concurrently with the actual process*

being performed (**Sonderman**: at least in Col.3 Lines 50-67; Col.7 Lines 8-20; at least in Col.4 Lines 48-64; Fig.1-8; Col.2 Lines 10-17).

Sonderman & Jain does not explicitly teach building an empirical model and using the first principle simulation results along with the empirical model to control the process performed by the semiconductor-processing tool. Empirical model & library as understood from the specification ([0078]) is the database of the simulation results, which provides "statistically sufficient sample of the parameter space".

Chen teaches creating an empirical model as disclosed in the specification as a statistical model built based on run-to-run or batch-to-batch results and using the results to control the process performed by the semiconductor-processing tool as well as to the next simulation step (Chen: Col.3 Lines 12-47; Col.6 Lines 34-67).

Arguendo, even if **Sonderman and Jain & Chen** do no explicitly teach said first principles simulation result being produced in a time frame shorter in time than the actual process being performed **Tan** teach the above limitation.

Tan *teaches said first principles simulation result being produced in a time frame shorter in time than the actual process being performed as in Col.2 Lines 7-12 as:*

(4) Model-based real-time process control using in situ inputs, process models, and process control strategies to correctly process control parameters during the process run, ensuring that product characteristics are achieved.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **Jain** to **Sonderman** to solve differential equation for the semiconductor processing tool. **Sonderman** teaches

building various models, which work in real-time feedback control simulating actual semiconductor modeling process (**Sonderman**: Fig.1; Col.7 Lines 8-20), while **Jain** makes possible by providing model-solving capacity in real time when differential equations are present in the model (like thermal patterns in semiconductor wafer model) (**Jain**: Abstract).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **Chen to Sonderman.** The motivation to combine would have been that Chen and Sonderman both are analogous art concerned with simulating the semiconductor fabrication process and providing the best control parameters to the actual semiconductor-processing tool (Chen: at least in Col.3 Lines 19-23).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **Tan** to **Sonderman** to facilitate the simulation as defined in Fig.2. The motivation to combine is that both **Tan** and **Sonderman** teach performing simulation of semiconductor assembly line including the tools and the processes running on them (**Tan**: Col.5 Line 63-Col.6 Line 8; **Sonderman**: **Sonderman**: Col.7 Lines 4-7; Col.3 Lines 56-63, Fig.1-3).

Regarding Claim 2

Sonderman teaches directly inputting the *process* data relating to the *actual* process *being* performed by the semiconductor-processing tool from at least one of physical sensor (eg. Scatterometry data, overlay data, dimensional data) and a metrology

tool physically mounted on the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 31-48; Col.4-8; Fig.1, 7; *Col.7 Lines 8-20*).

Regarding Claims 3-5

Sonderman teaches indirectly inputting the *process* data relating to the *actual* process performed by the semiconductor-processing tool from one of the manual input devices and a database as manual fashion data retrieval and automatic data retrieval; inputting data recorded from the previous run; inputting the data set by a simulation operator (Sonderman: at least in Fig.1-3 Col.1; Col.4-7; Col.7 Lines 8-20).

Regarding Claims 6-7, 9

Sonderman teaches inputting process data relating to at least one of the physical characteristics of the semiconductor-processing tool and semiconductor tool environment, data relating to at east on of the characteristics and a result of a process performed by the semiconductor processing tool; inputting fundamental equations necessary to perform first principle simulation for the desired simulation result (**Sonderman**: at least in Col.5 Lines 10-18; Col.6 Lines 48-63; Col.9 (equations); Col.5-9; Fig 1-3; Col.7 Lines 8-20). **Sonderman** and **Jain** teach inputting fundamental equations as the set of computer encoded differential equations (**Sonderman**: Col.9 (equations); **Jain**: Pg. 372 Section V Dedicated MPE, Abstract).

Regarding Claim 10

Sonderman teaches performing interaction concurrently between the simulation environment (first principle simulation) and the semiconductor-processing tool (Sonderman: Fig.2; Col.4 Lines 48-63).

Regarding Claims 11

Sonderman teaches performing first principle simulation independent of the process performed by the semiconductor-processing tool (Sonderman: at least in Col.5-8; Fig.3-6 especially col.7).

Regarding Claim 14

Sonderman teaches using the first principles simulation result comprises using the first principles simulation result to perform at least one of detecting, and classifying a fault in the process performed by the semiconductor-processing tool (Sonderman: at least in Col.5 Line 56 – Col.6 Line 24).

Regarding Claims 15-19

Sonderman teaches using a network of interconnected resources inside the semiconductor manufacturing facility (Sonderman: Semiconductor tools on the factory floor – Col.9 Lines 60-65) to perform first principle simulation (Jain: Section III) recited in claim 1; using code parallelization among interconnected computational resources to share the computational load of the first principle simulation (Sonderman: Fig.1-3, computer code software is described in Col.9 Lines 58 onward; Col.5-8); sharing simulation information among the interconnected resources to facilitate a process by the semiconductor-processing tool (Sonderman:

Fig.1-3, computer code software is described in Col.9 Lines 58 onward; Col.5-8; Sonderman: Col.1 Lines 42-62 - APC resource Col.9 Line 58- Col.10 Line 20); sharing simulation results among the interconnected resources to reduce redundant execution of substantially similar first principle simulation by different resources (Sonderman: Fig.1-3, computer code software is described in Col.9 Lines 58 onward; Col.5-8; Sonderman: Col.1 Lines 42-62 - APC resource Col.9 Line 58- Col.10 Line 20); sharing information comprising model changes among the interconnected resources to reduce the redundant refinements of first simulation by different resources (Sonderman: Col.1 Lines 42-62; Sonderman: Col.1 Lines 42-62 - APC resource Col.9 Line 58- Col.10 Line 20).

Regarding Claims 20-21

Sonderman teaches remote access to computational and storage resources (Sonderman: Col.9 Line 58-Col.10 Line 31) where in wide area network is art inherent.

Regarding Claim 23

Sonderman teaches first principle simulation controlling at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace (Sonderman: at least in Col 4 Lines 18-31; Col.3 Lines 45-49).

Regarding Claim 24

Chen teaches first principle simulation controlling a chemical vapor deposition (CVD) system (Chen: Col.7 Line 43-55 – simulation controlling actual process/equipment; Col.1 Lines 2-5 CVD as actual equipment; Col.6 Lines 34-51 – simulation w/ actual process).

Regarding Claim 25

Sonderman teaches inputting various parameters relating to etching, deposition etc. (Sonderman: at least in Col.5 Lines 56-67)

Regarding Claim 26

Sonderman teaches inputting physical geometric data as parameters for the equipment model where the equipment could be at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace (Sonderman: Col.5 Lines 56-67).

Regarding Claim 27

Sonderman teaches first principles simulation result controlling the semiconductor processing tool by using model output to adjust said process performed by the semiconductor processing tool (Sonderman: Col.4 Lines 48-64; Fig.1-2).

Regarding Claim 28-34

System claims 28-34 disclose similar limitations as claims 1-7 and are rejected for the same reasons as claims 1-7 respectively. Sonderman discloses an input device (Sonderman: Fig.1 Elements 180, 210 and 130).

Regarding Claim 36-38

System claims 36-38 disclose substantially similar limitations as method claims 9-11 and are rejected for the same rationale as claims 9-11 respectively.

Regarding Claims 41-48

System claims 41-48 disclose substantially similar limitations as method claims 14-21 and are rejected for the same rationale as claims 14-21 respectively.

Regarding Claims 50-54

System claims 50-54 disclose substantially similar limitations as method claims 23-27 and are rejected for the same rationale as claims 23-27 respectively.

Regarding Claim 58

System claim 58 discloses substantially similar limitations as method claim 1 and is rejected for the same reasons as claim 1.

Regarding Claims 59-60

Jain teaches use of Navier Stokes and other known simulation solutions (reuse) for solving various simulation problems as initial condition (Jain: Pg. 367-368 Section "Governing Rationale" Sub-Section A. Governing Equations). Sonderman also teaches initializing the models with input data (Sonderman: Col.7 Lines 8-20).

4. Claims 22 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sonderman, in view of Jain, in view Chen, in view of Tan, further in view of IEEE article "Heat Analysis on Insulated Metal Substrates" by Naomi Yunemura et al (Yunemura hereafter).

Regarding Claim 22

Teachings of *Sonderman, Chen, Jain* and Tan are disclosed in claim 1 rejection above. Sonderman also teaches that the first principle simulation models the equipment conditions, thereby modeling temperature response and pressure response during various processes (Sonderman: at least in Col.5 Lines 62-67). *Sonderman, Chen Jain* and Tan do not teach explicitly that such temperature and pressure modeling is done using ANSYS computer code. *However, Jain teaches SIMD based processing to solve the computer-encoded differential equations (Jain: Pg. 370 Section III Parallel architectures for solving PDE).*

Yunemura teaches that heat simulation modeling can be performed using ANSYS computer code (Yunemura: Pg. 1407 Section 1) on a silicon chip.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Yunemura to Sonderman, Chen and Jain to create a equipment model as disclosed by Sonderman. The motivation to combine would have been that Yunemura teaches heat modeling on a silicon chip affecting the thermal conductivity (Yunemura: Pg.1407 Section 2) based on various thicknesses and Sonderman is solving the same issue for the equipment model that for example model the equipment for depositing the various layers and

affects on heat and pressure. ANSYS is known in art to be used as thermal & pressure modeling tool based on finite element analysis. Yunemura's teaching thereby facilitates computer-encoded differential equations solving which is considered to be prime issue by Jain (Jain: See Section III, Networking and Dedicated MPE's for solving the computer-encoded differential equations).

Regarding Claim 49

System claim 49 discloses similar limitations as claim 22 and is rejected for the same reasons as claim 22.

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Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AKASH SAXENA whose telephone number is (571)272-8351. The examiner can normally be reached on 8:00- 6:00 PM Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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